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Design and Analysis of 8T CMOS SRAM cell

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Abstract: This paper addresses to enhance the stability of8T SRAM bitcell by lowering its leakage power. Scaling down of process parameters such as supply voltage affects the Read ability and Write stability of the cell. As number of transistors on chip increases power dissipation also increases and as a result of this stability of the cell gets affected. This paper aims at reducing the leakage power and improving the static noise margin of the cell. Static Noise Margin (SNM) is defined as the maximum amount of noise that a circuit can withstand at its input without causing any change in its output. Cadence Virtuoso tool was used for simulation and simulations were done using 180nm technology model file.

Keywords: SNM, Cadence Virtuoso, 6T, 8T, leakage power, stability, Read margin, Write margin.

I. INTRODUCTION

Semiconductor memory units capable of storing large amount of digital data are heart of all the digital devices. Amount of memory required for particular system depends on the type of application it is used for. Applications such as high speed gaming requires a large amount of memory to work with.

In this technological era electronic devices are in huge demand and is need of everyday life. Multimedia applications such as mobile phones, PDA's, Laptops etc. requires a large amount of memory accesses to work with. SRAM (Static Random Access Memory) is fastest of all memories but in contradiction it is the most expensive one and takes up large amount of processors space. 256kb size of SRAM is equivalent to 1Mb of DRAM. As process technology is scaled down more and more transistors are incorporated on a single processor chip. This is proving to be advantageous in the manner that since device dimensions are shrinking customers can play with smaller size devices incorporating multiple features. But increase in number of transistors on chip area is also resulting in increase in power dissipation.

Present scenario depicts that the number of transistors required for storing the digital information is greater compared to that required for performing the logic operations. Increasing demand for large data storage memory arrays has driven the fabrication technology and memory development to come up with more compact design rules. These rules help thedesign engineers to build a compact yet large storage capacity memory cell.

Memories are divided into two types; Volatile memories and non-volatile memories. Volatile memories are one which can retain its data only as long as the power is supplied to it whereas non-volatile memories are the one which does not require continuous power to retain its data. Volatile memories are categorized as Random access memory (RAM) and Read only memory (ROM).RAM is further divided into Static RAM (SRAM) and Dynamic RAM (DRAM).SRAM retains it data only as long as the power is supplied to it which is in contrast to DRAM which needs to be refreshed quite a many times but does not require continuous supply for retaining the digital information. DRAM stores the data bit as a charge in capacitor whereas SRAM flips the data bit whenever data need to be written inside the storage cell. Memory array organization is as shown in fig 1.

SRAM cell array is fastest of all the memory arrays but in contrary is bit expensive compared to any other unit.As per Market analysis firm, Semico Research predicts that by 2017, nearly 70% of SoC's die area will be taken up with SRAM. [2]Therefore inorder to reduce the power dissipation and also the cost most of the researchers are focusing on designing a low power on chip memory array. Operation of SRAM cell is affected by random process variation and this issue becomes prominent in Nano-scaled technology thereby degrading the stability of cell. Scaling down of process parameters such as supply voltage (VDD) and increase in variability affects the stability of the cell.

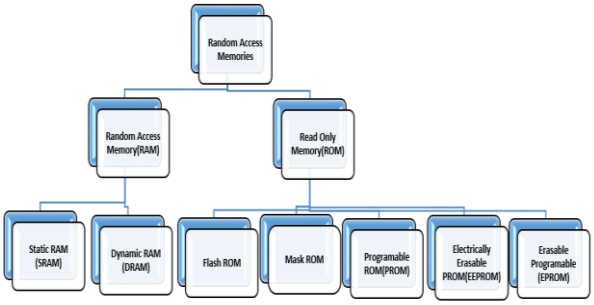

Fig 1.Memory array organization

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Static Noise Margin (SNM) is defined as the maximum amount of noise that a circuit can withstand at its input without causing any change in its output. Scaling down of device parameters such as supply voltage scaling makes circuit sensitive to process variations such as dopant fluctuations thereby affecting the stability of cell. This topic of research is becoming a challenge for design engineers since reduction in power supply reduces the static power dissipation of the cell.

II. 6T SRAM ARCHITECTURE

Fig 2 shows architecture of conventional 6T SRAM cell. It consists of six transistors, a word line (WL) and a bit line (BL). Four Transistors M1, M2, M3, M4 forms two cross coupled inverters (storage cell) that stores either bit '1'or bit '0'. Other two transistors M5 and M6, also termed as access transistors are used to access the storage cell depending on whether the word line (WL) is set to logic high(1) or logic low(0). If WL is set to '1'than the storage cell can be accessed, otherwise it remains isolated from the circuit.

W power

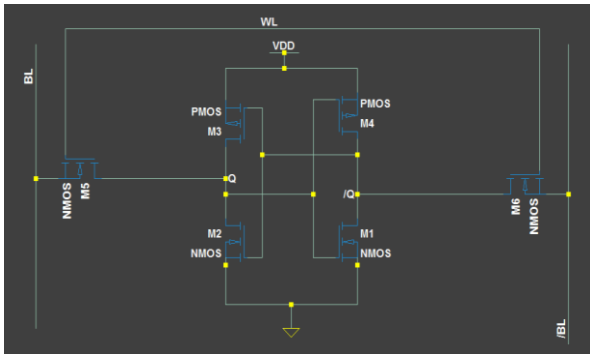

Fig 2. Schematic of conventional 6T SRAM cell

During standby mode WL is set to logic low (WL=0). Therefore no memory storage cell can be accessed at this time. Read operation is carried out by asserting the word line. This turns on the access transistors M3 and M4 thereby connecting the bit lineswith storage cell. Both BL and BLB are pre-charged to VDD. Sense amplifier senses the differential voltage between bit linesand depending on the stored value in the storage cell corresponding bitline is discharged. If stored value was '0' then BL discharges else BLB will discharge. To carry out write operation, assume that cell is originally storing a '0' and we wish to write a '1'.To accomplish this BL is pre-charged to VDD and BLB is set to 0V.The cell is selected by raising WL to VDD. When word enable WE goes high ,value of output 'Q' is flipped from '0' to '1' and write operation is accomplished.

Read/ write operation with Q/Qbar transitions are as as shown in figure 4.

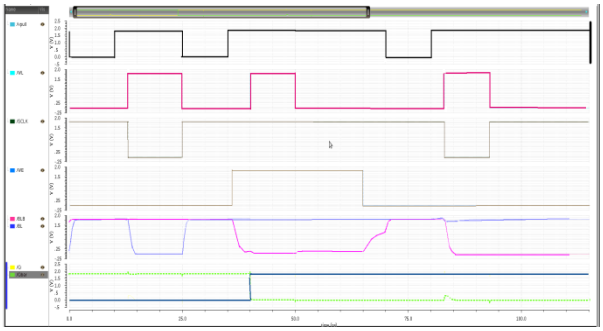

Fig 4.Simulation results for 6T SRAM cell

III. DIFFERENTIAL SINGLE PORT 8T SRAM CELL

Most widely used differential ended 8T bitcell requires more chip area compared to conventional 6T SRAM cell since it uses two separate ports for performing read and write operation. In Differential ended dual port 8T bitcell read and write ports can be accessed simultaneously, but this causes the read disturbance because bitcell current decreases when read and write ports access the same row at the same time [2]. At low voltages single ended structure improves the stability of bitcell but gives poor noise immunity [3].

Differential ended single port SRAM gives better noise immunity compared to single ended design

This cell consists of eight transistors, word line (WL) and a bit line (BL). Sources of transistors M7 and M8 are connected to Control (CNTRL) and Control-bar (/CNTRL) which changes its role accordingly.

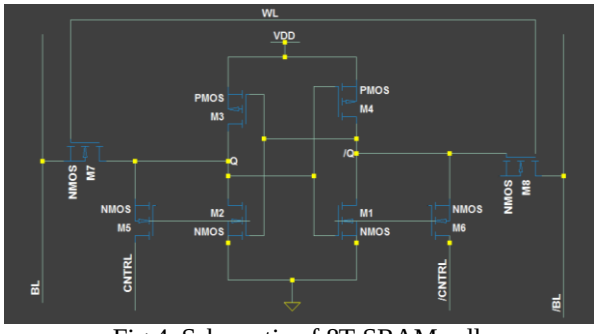

Fig 4. Schematic of 8T SRAM cell

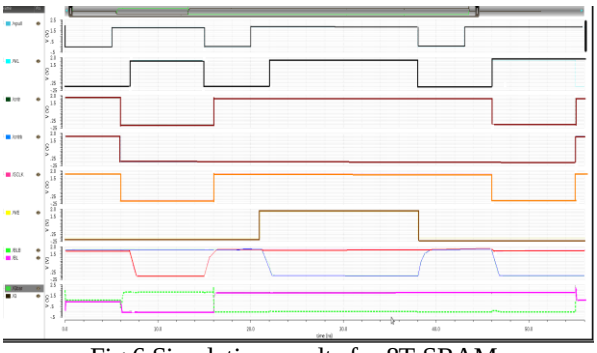

Fig 6.Simulation results for 8T SRAM

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During read operation CNTRL and /CNTRL are connected to ground inorder to achieve fast discharging of bitline. On the other hand these signals are connected to voltages same as that of bitlines inorder to achieve write operation.

IV. DISCUSSION

SNM of 6T and 8T cell was found at 1.8 V through spectre simulator using the cadence gpdk 180nm technology. All transistors were designed with a minimum width of 50um and default supply voltage (VDD) of 1.8V.

Time taken by bit line to charge during read operation by conventional 6T SRAM cell was found to be 30ns ns and for discharging it was found to be 11ns and for 8T it was found to be 15ns and 8ns respectively.

Author is currently working on design of novel 8T SRAM cell that will give improved stability compared to conventional SRAM.

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REFERENCES

[1] CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies (Frontiers in Electronic Testing, 2008) by Andrei Pavlov, ManojSachdev.

[2] Y. Ishii, Y. Tsukamoto, K. Nii, H. Fujiwara, M. Yabuuchi, K. Tanaka, S. Tanaka, and Y. Shimazaki, "A 28 nm 360ps-access-time two-port SRAM with a time-sharing scheme to circumvent read disturbs," in IEEE Solid-State Circuits Conference (ISSCC), pp. 236 – 238, Feb. 2012.

[3] Samira Ataei and James E.Stine "A Differential Single-Port 8T SRAM bitcell for Variability Tolerance and Low Voltage Operation",Oklahoma State University, 978-1-5090-0172-9/15/$31.00 c 2015 IEEE.

[4] DRAM circuit design- a tutorial-IEEE (2001) (IEEE Press series on microelectronic systems) by Brent Keeth R Jacob Baker.

[5] Ashok K. Sharma, "Semiconductor memories Technology Testing and reliability".

[6] Jay Narayan, R.K.Sharma- NIT Kurukshetra "A Novel Single Ended 8T SRAM with Improved Noise Margins and Stability" Proceedings of 2014 RAECS UIET Panjab University Chandigarh, 06 - 08 March, 2014

[7] AlifVaknin, OrtalYona, Adam Teman"A Double-Feedback 8T SRAM Bitcell for Low-Voltage Low-Leakage Operation" 978-1-4799-1361-9/13/$31.00 ©2013 IEEE

[8] Lecture - 31 Design of Memory Circuits, Indian Institute of technology Kharagpur - YouTube